EcoInfo

"Vers une informatique éco-responsable ?"
23 avril 2015 – CNRS Paris Michel Ange

Transistor MOS ultime et autres pistes pour le futur de la microélectronique sur silicium

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Aix*Marseille université

Plan de l'exposé

- **Introduction : microélectronique sur silicium**
  Le marché de la microélectronique, loi de Moore

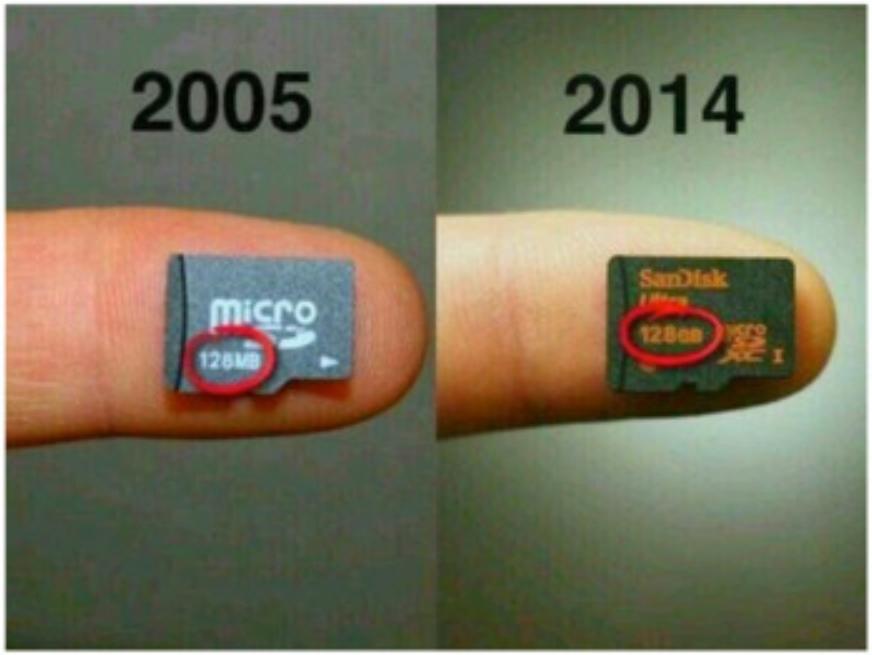
- **Le transistor MOS, brique de base des circuits intégrés**
  Fonctionnement et performances du dispositif

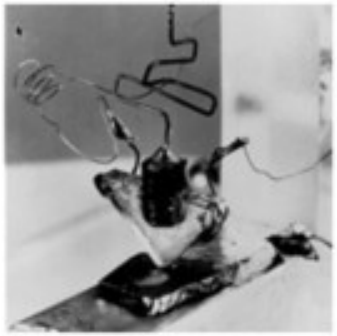
- **Les limites du transistor MOS sur silicium massif**
  Problèmes de réduction d'échelle

- **Architectures innovantes : nanoélectronique sur silicium**
  « More Moore »

- **Et ensuite ?**
  « More than Moore » & « Beyond CMOS »

Introduction





LE TRANSISTOR & LE CIRCUIT INTEGRE
OBJETS TECHNOLOGIQUES DU XX^{e} SIECLE !

A l'origine de plusieurs « révolutions »:
technologique, économique, sociétale,…

ORDINATEUR, TELEPHONIE MOBILE
INTERNET, PHOTOGRAPHIE,…

des changements radicaux, totalement imprévus,
extrêmement rapides, et globaux

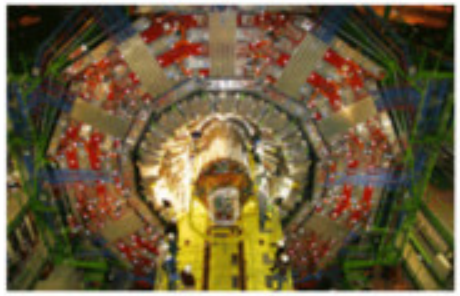
Hier (1970) : un monde sans microélectronique

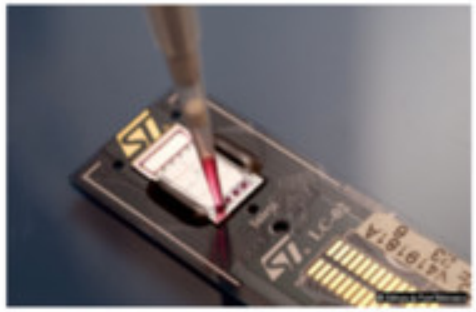
Aujourd'hui (2015) : une microélectronique omniprésente





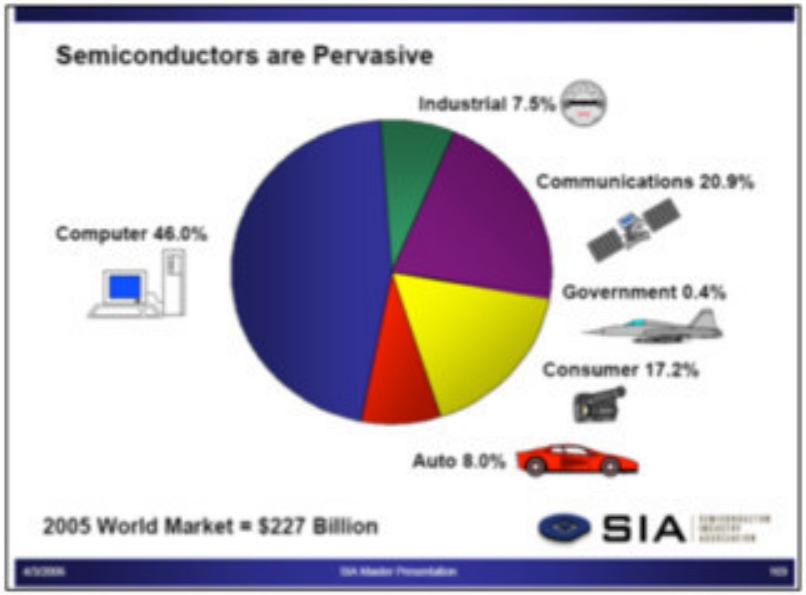


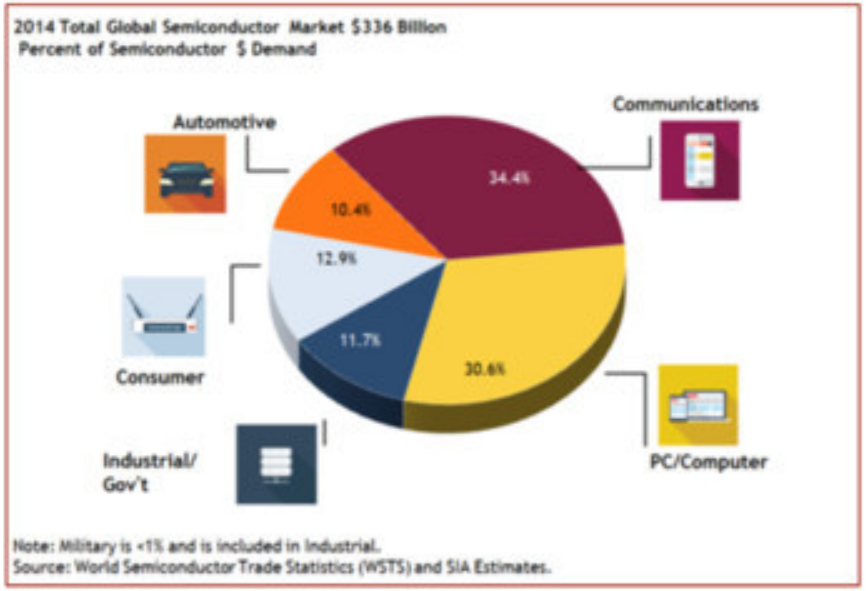



Un marché croissant (+7%/an) en constante évolution

2005 : $ 227 B



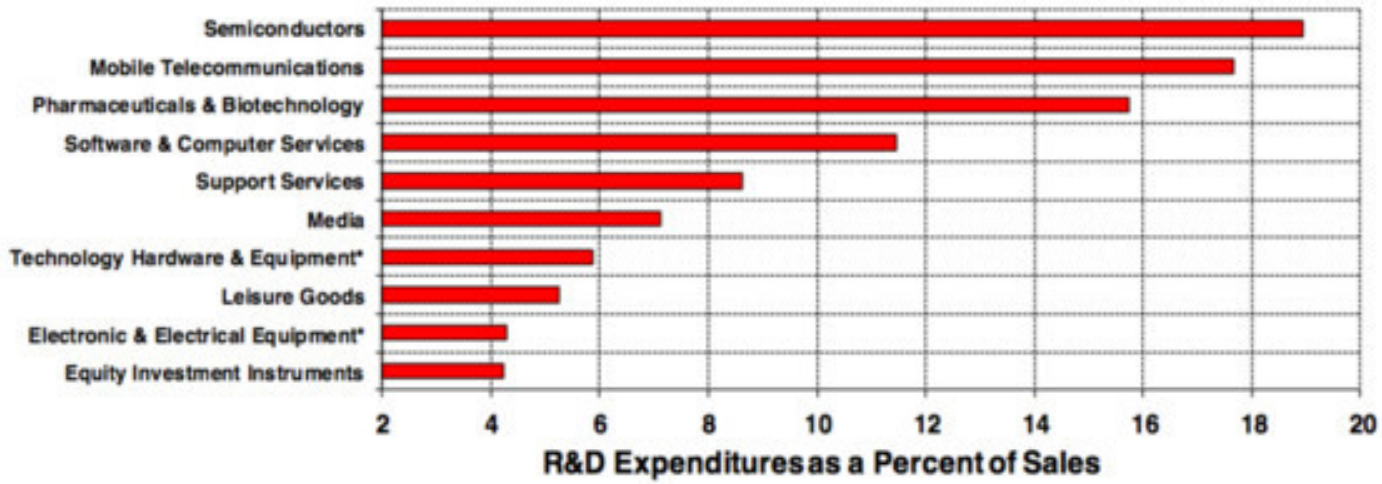
2014 : $ 336 B

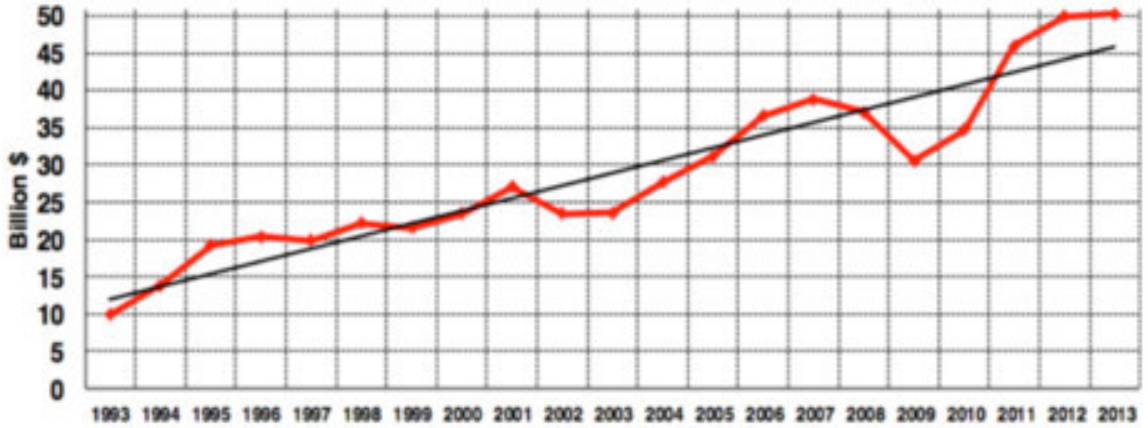


Innovation ➔ Nouveaux produits ➔ Nouveaux marchés

Source: www.semiconductors.org/

Un effort de R&D sans équivalent



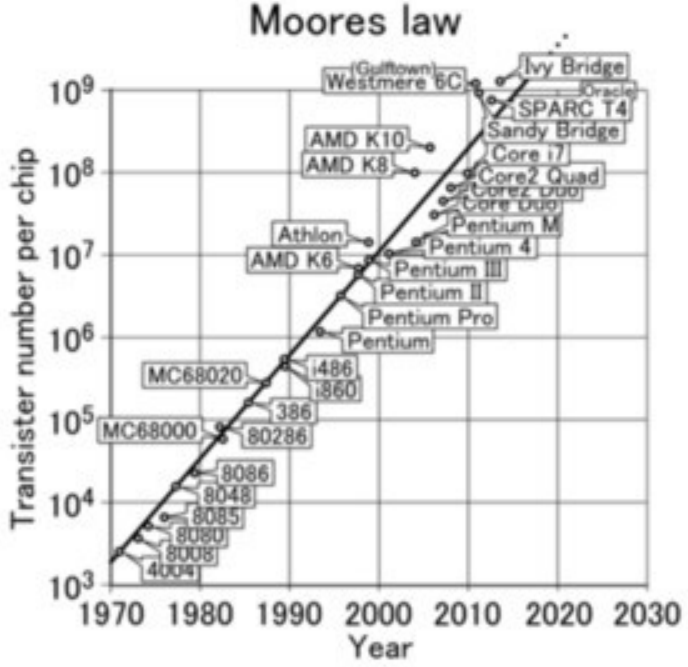


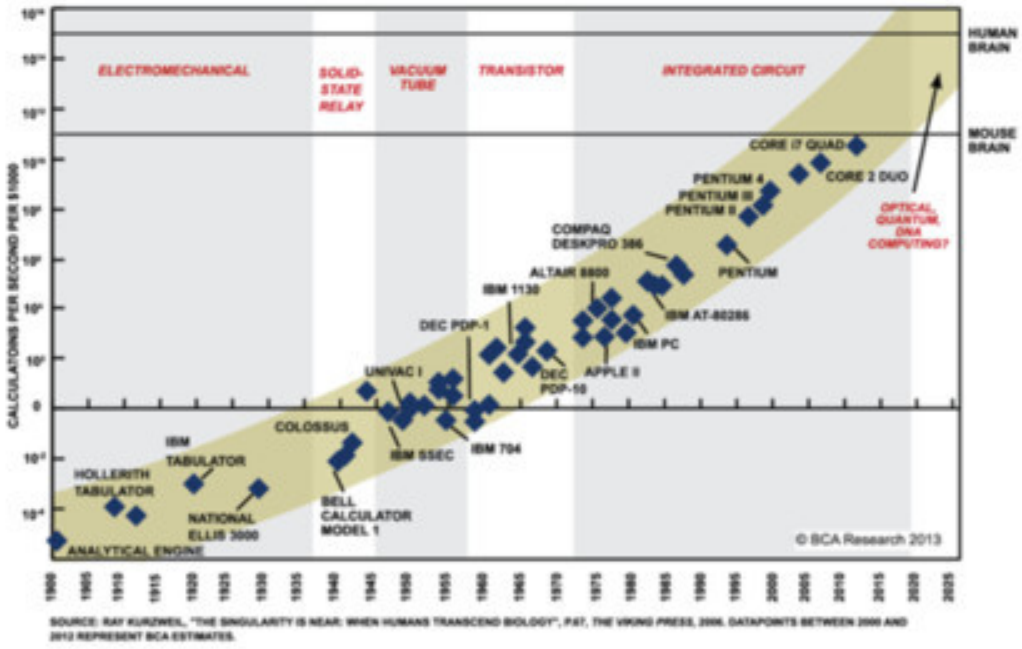
Source: SIA factbook 2014

« Loi » de Moore

MOORE'S LAW 50 YEARS

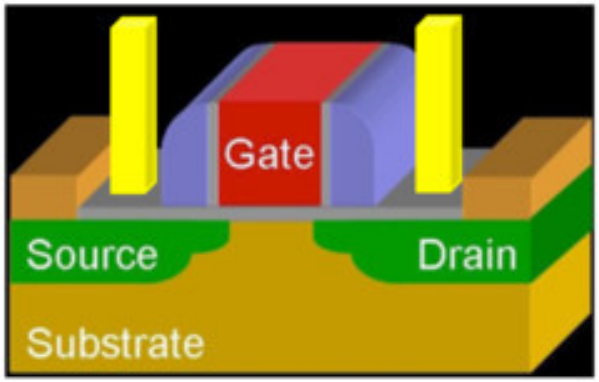
« le nombre de transistors des processeurs devrait doubler tous les 18 mois et permettre ainsi une croissance exponentielle régulière des performances » - Gordon Moore (Intel) - 1965

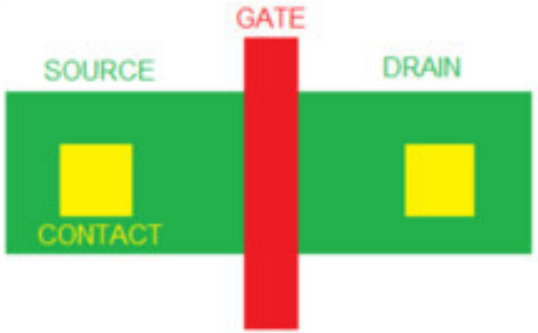


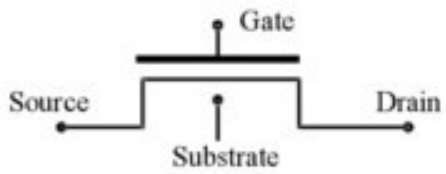


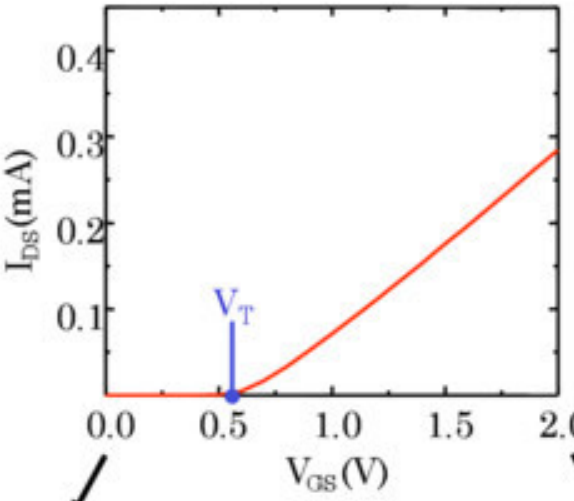
Le transistor MOS,
brique de base des circuits intégrés

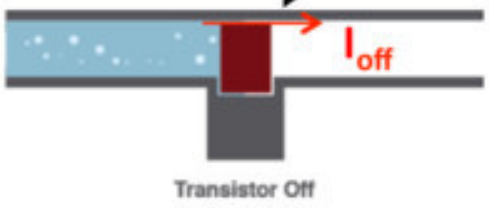
Le transistor MOS

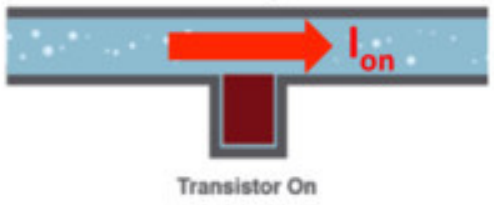




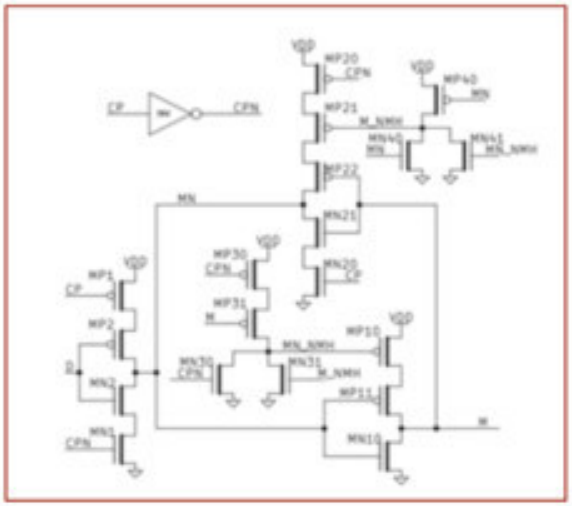


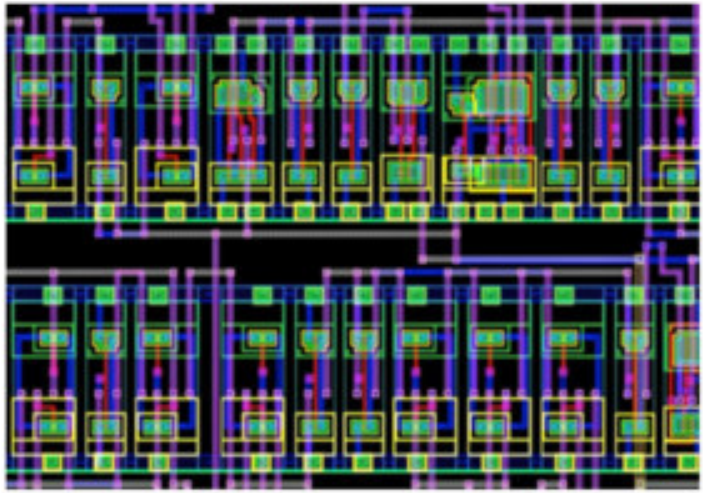


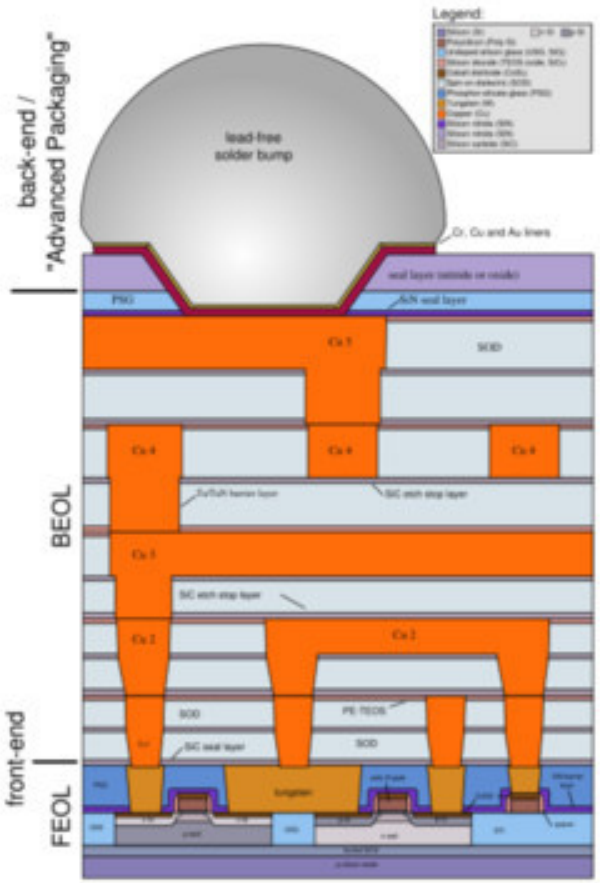




Circuit intégré = interconnexion de transistors MOS

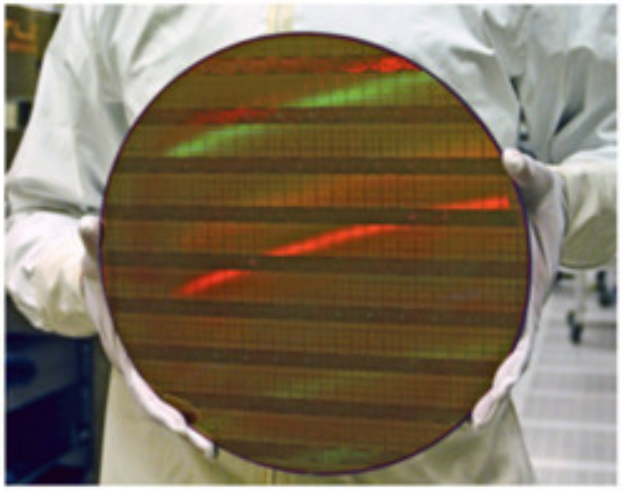






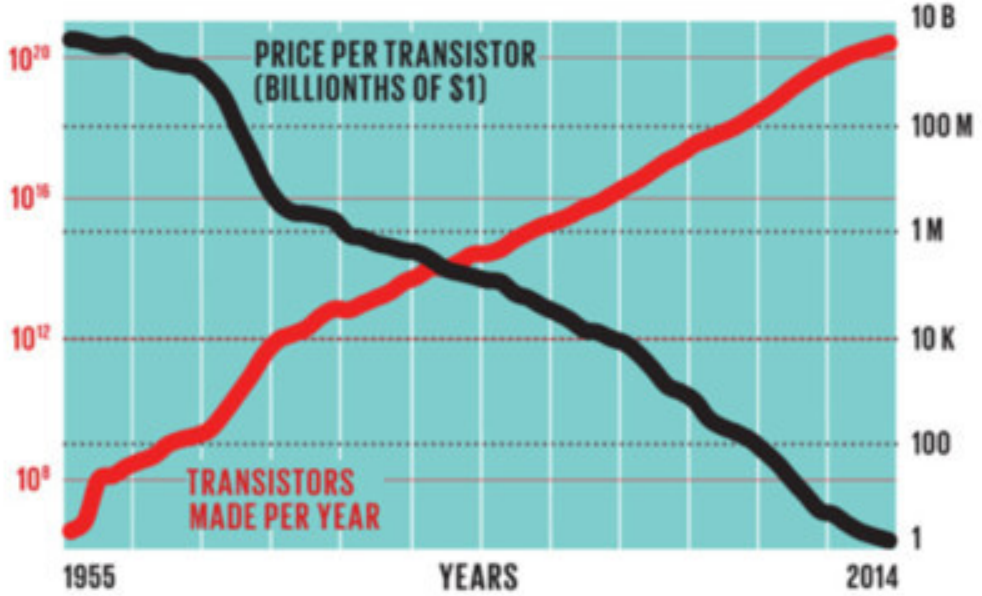
Le transistor MOS

L'objet technologique le plus fabriqué dans le monde : 2.5×10^{20}/an en 2014.
Chaque seconde, 8000 milliards de transistors MOS sont fabriqués (sur Terre).



Source: Intel

Procédés microélectroniques : fabrication collective sur wafers



Source: IEEE Spectrum 2015

≈ 180 millions de wafers/an (équivalent 200 mm)
≈ 6 millions de m^2 de silicium manufacturé/an

Le transistor MOS

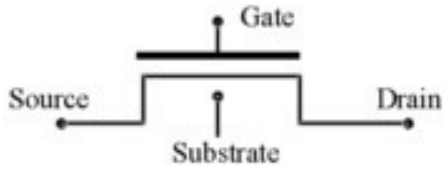
Longueur de canal

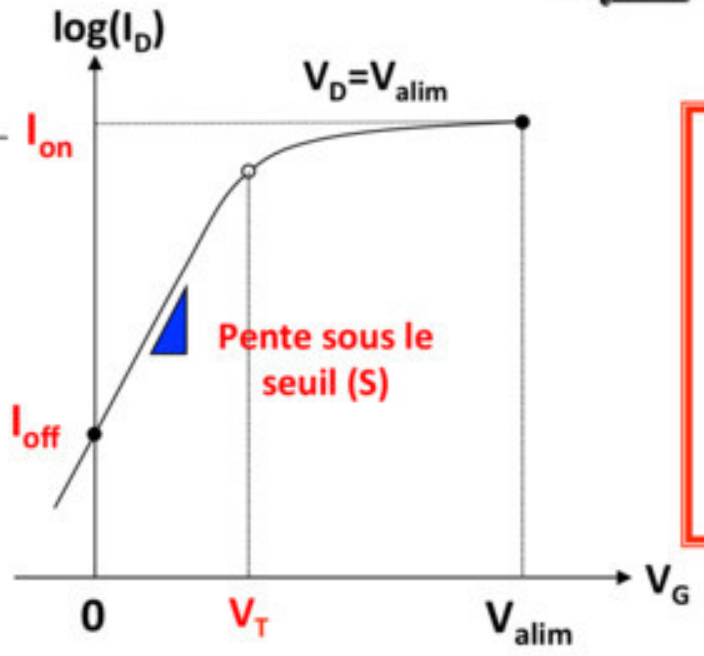
Tension d'alimentation

$$\frac{I_{on}}{W} = \frac{1}{L}\mu_n C_{ox}\left[V_G - V_T - \frac{V_D}{2}\right]V_D$$

Mobilité des porteurs (transport électronique dans le matériau de canal)

Charge d'inversion (couplage électrostatique grille-canal)





Transistor "idéal"

- $I_{on} \rightarrow \infty$
- $I_{off} \rightarrow 0$
- $1/S \rightarrow 0$
- $0 < V_T < V_{alim}$

⇒ **Conséquences au niveau circuit**

"Switching delay" on state → off state

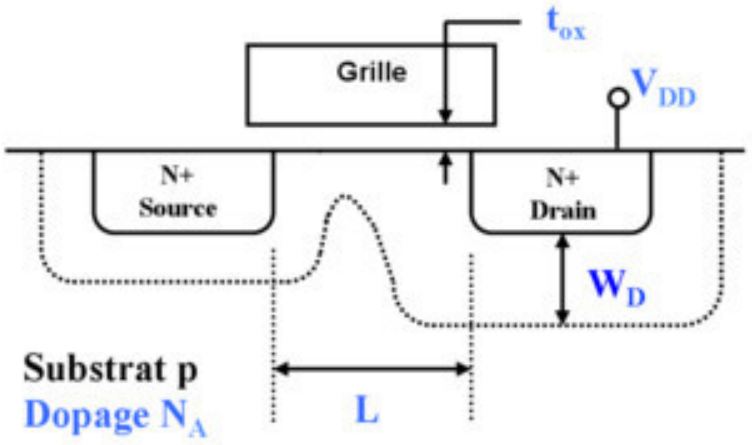
$$\tau \propto \frac{CV_{supply}}{I_{on}}$$

Principe de réduction d'échelle du transistor MOS

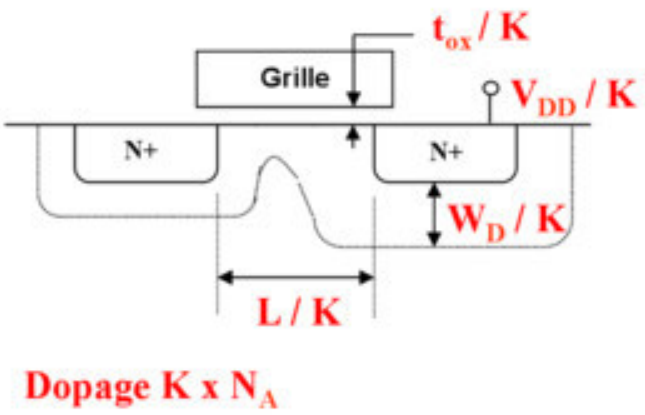
- **Dennard et al. (1974)**

- **Principe :** ***réduction des tensions appliquées et des dimensions du dispositifs par le même facteur K, afin de conserver le champ électrique***

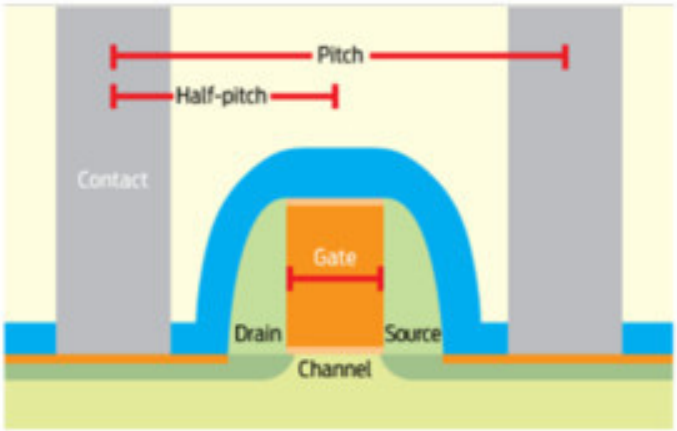
Transistor initial (long)

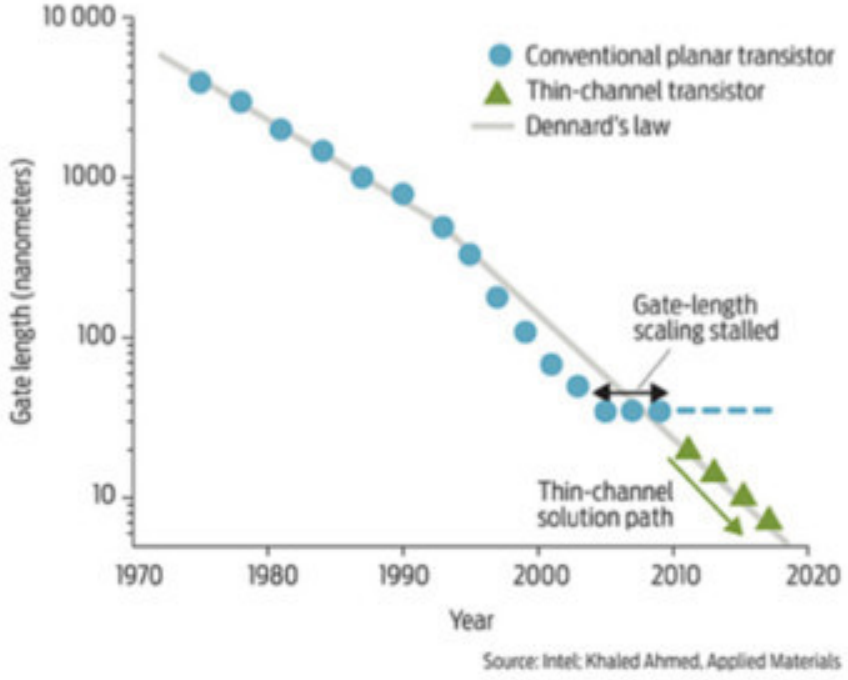


Transistor réduit (court)



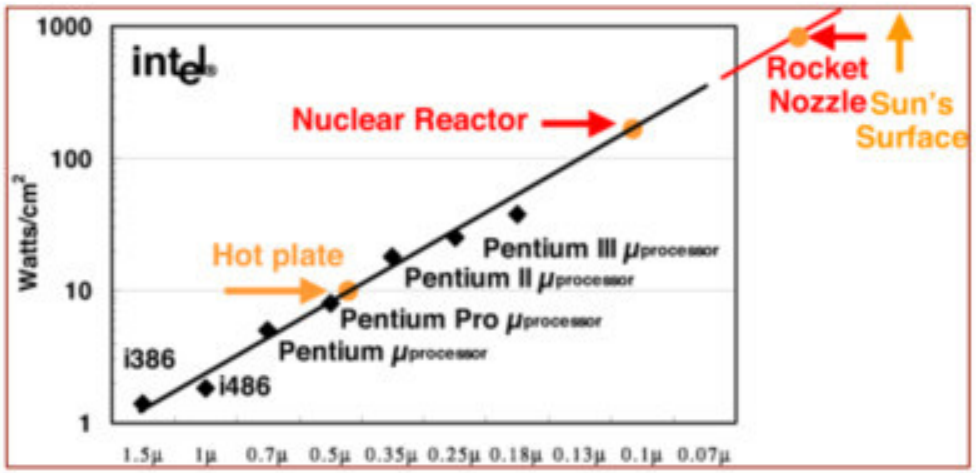
Nœuds technologiques

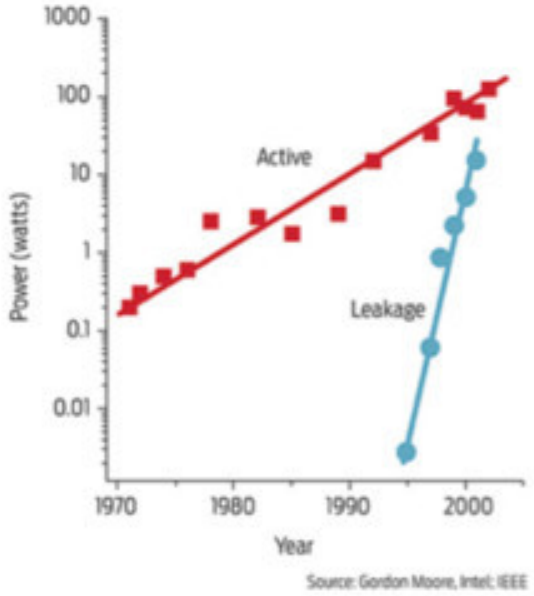




Principe de réduction d'échelle du transistor MOS

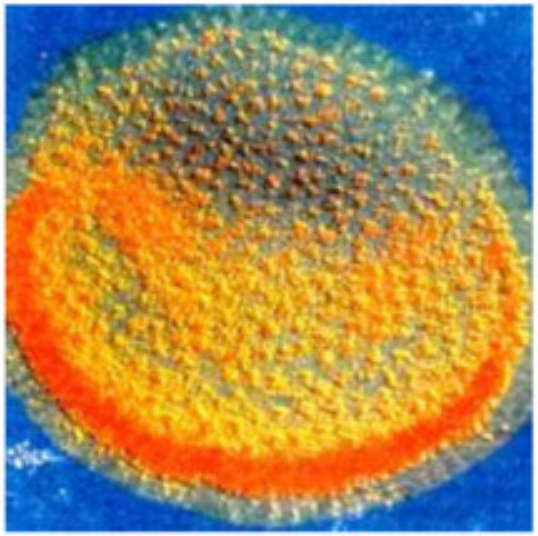
- **Baccarani et al. (1984)**
- **Principe :** *la tension d'alimentation n'est plus réduite dans la même proportion que les dimensions*
- **Facteur additionnel $\alpha > 1$ pour le champ électrique**



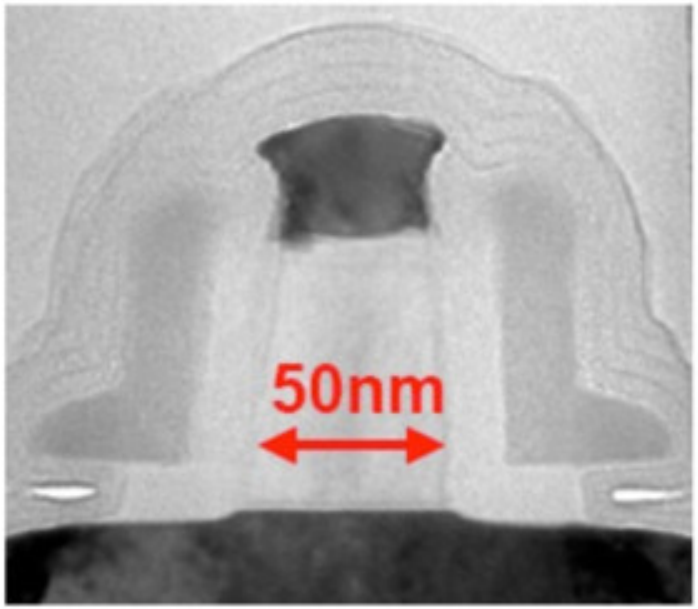


Les limites du transistor MOS sur silicium massif (bulk)

Virus de la grippe

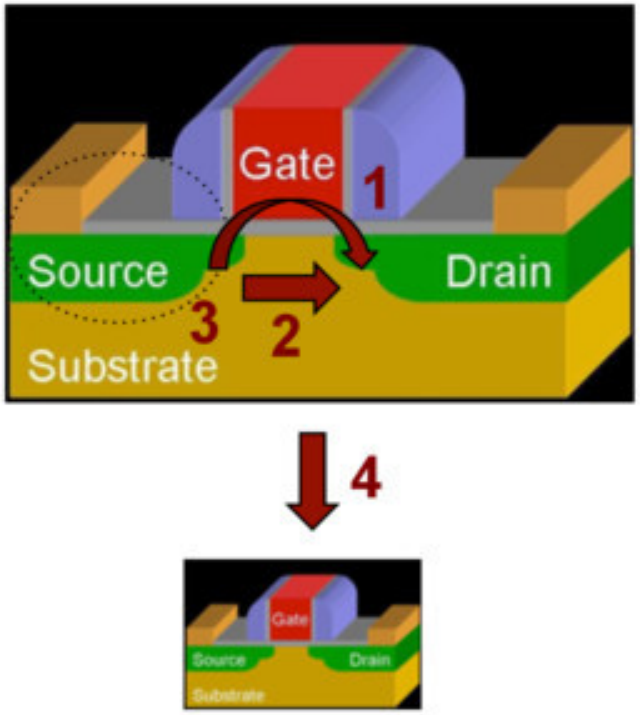


Transistor 90nm (Intel®)



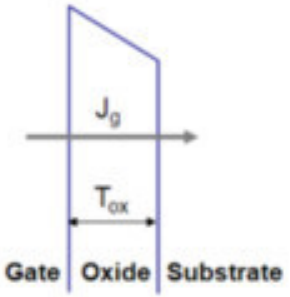
Source: Intel

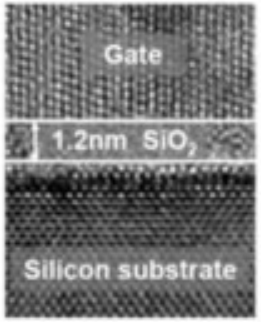
Principales limitations du transistor MOS bulk

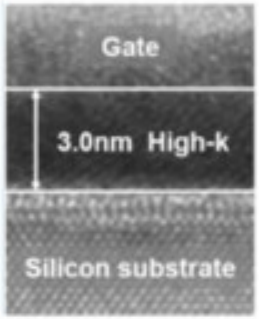


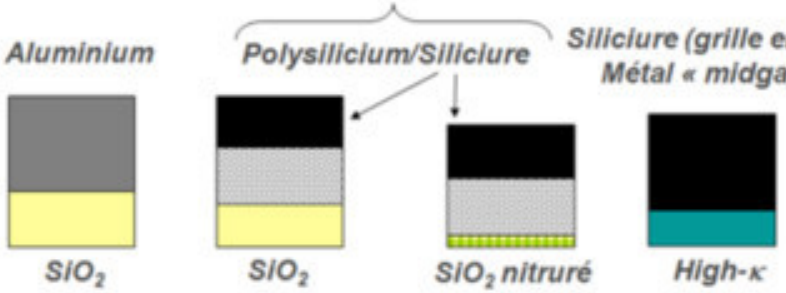
1. **Electrostatique**
   - Couplage grille-canal – Effets de canaux courts
   - Courant source-drain à l'état OFF
   - Courant de fuite de grille (tunnel)
2. **Transport électronique**
   - Mobilité des porteurs de charge
   - Courant à l'état ON
3. **Impédances parasites**
   - Résistances d'accès au canal
   - Capacités parasites
4. **Phénomènes physiques émergents**
   - Effets de confinement quantique
   - Transport non-stationnaire
   - Transport Balistique
   - Fluctuation des dopants

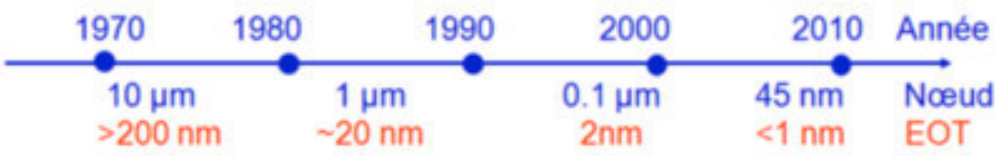
Courant de fuite tunnel – Introduction des matériaux high-κ

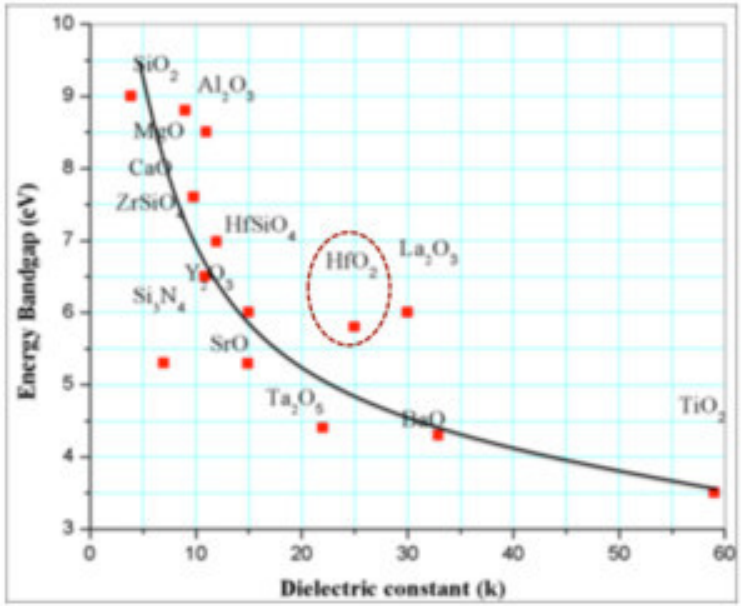








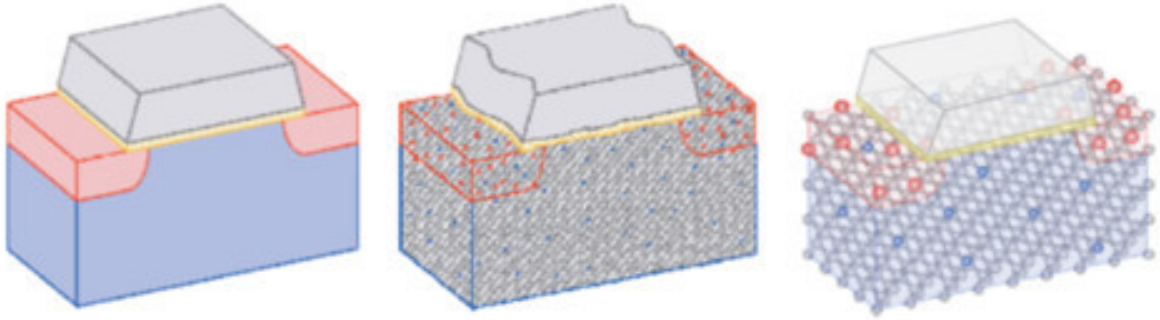




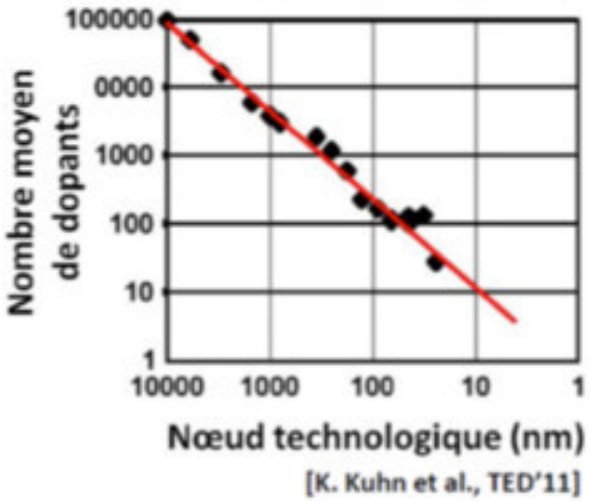
➔ **Problème potentiel : épuisement des ressources d'hafnium**

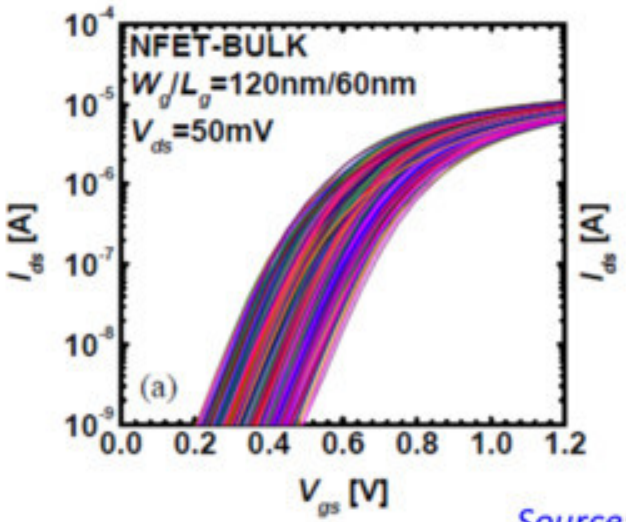
72
Hf
Hafnium
178.49

Variabilité stochastique du V_T sur silicium massif



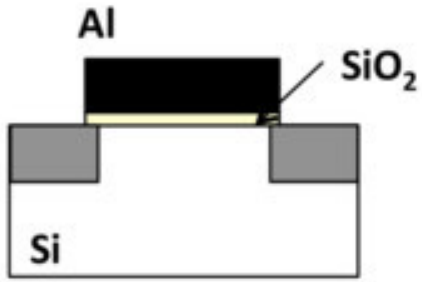
Traditional 22 nm Sub-10 nm



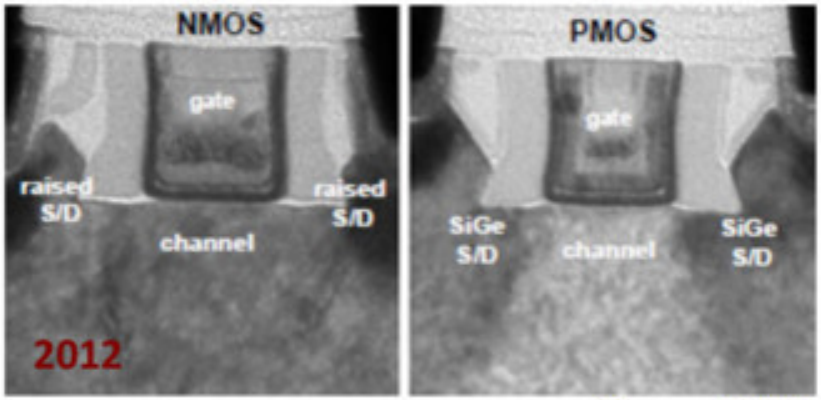


Source: CEA-LETI

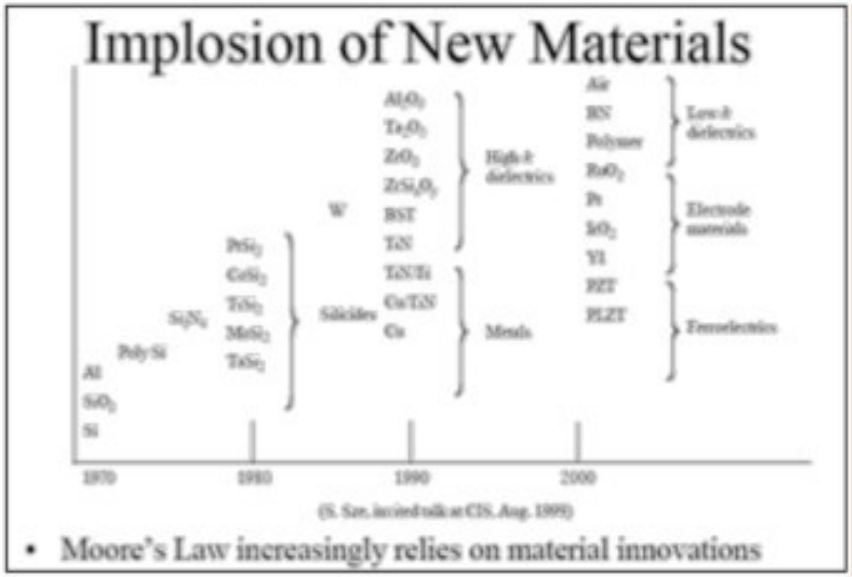
Le transistor MOS bulk poussé à ses limites

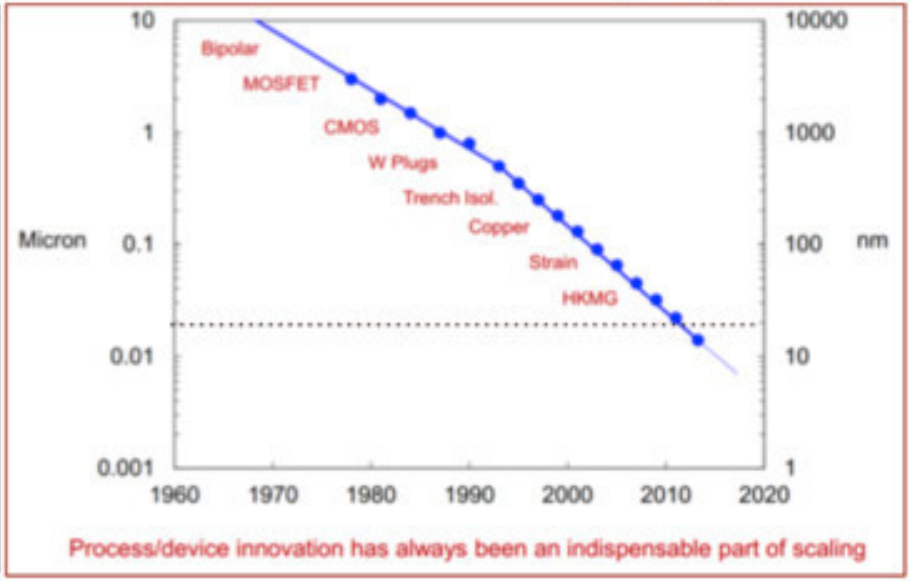


1971



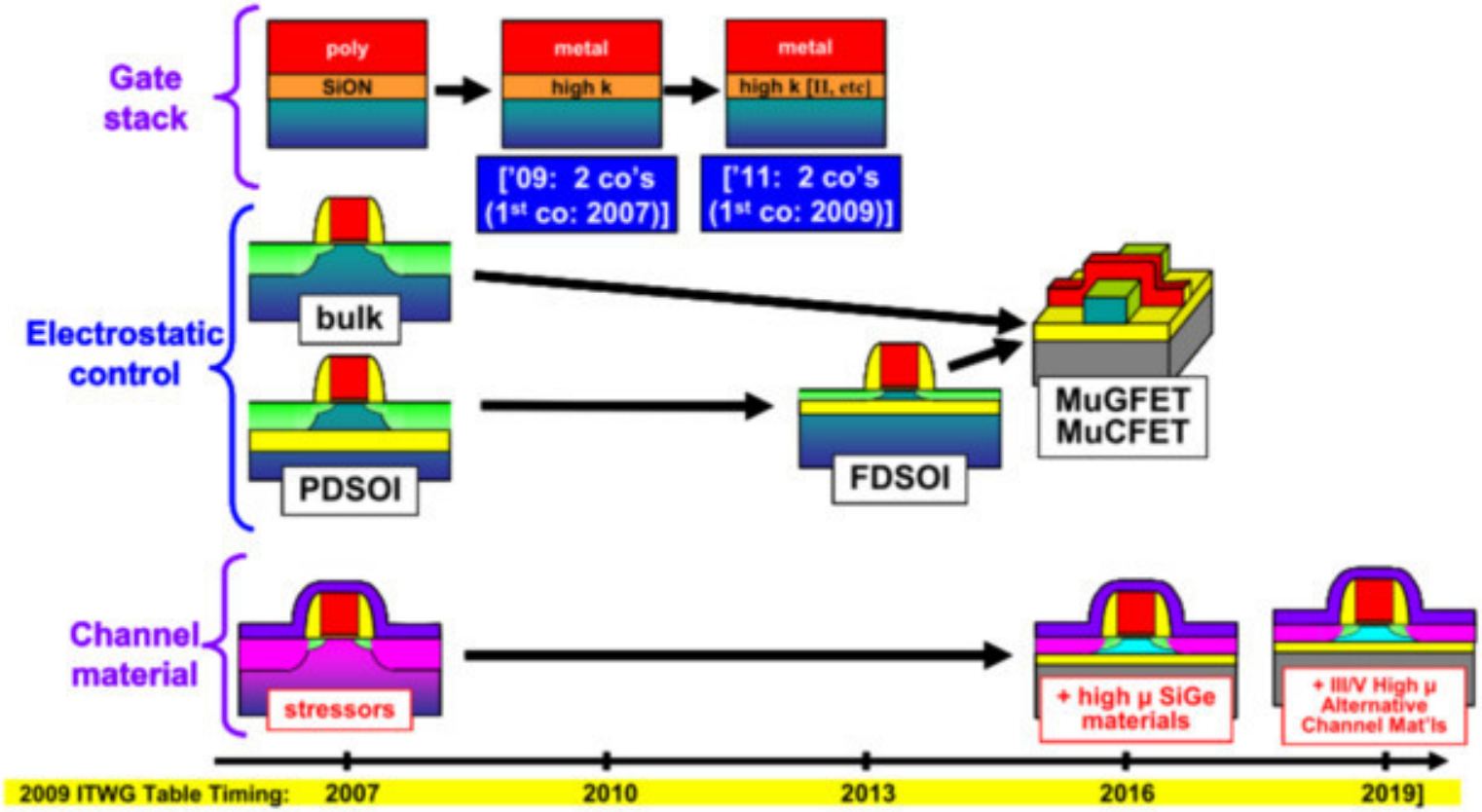
Source: Intel





Architectures innovantes : nanoélectronique sur silicium

Architectures innovantes et nouveaux matériaux: « More Moore »



Architectures innovantes et nouveaux matériaux: « More Moore »

No end in sight for logic scaling

N20

Bulk CMOS:
Complementary Metal Oxide Semiconductor

N20 / N14

SOI:
Silicon on Insulator

N1x / N7

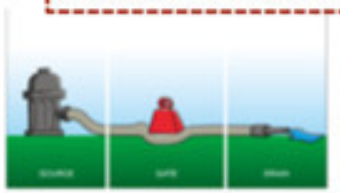
Bulk FinFet :
Fin field effect transistor

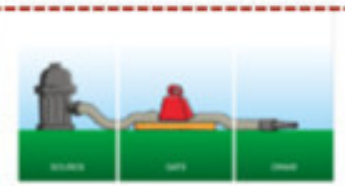
N7 / N5

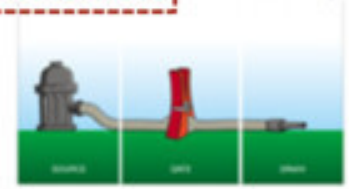
SOI FinFet :
Silicon on insulator fin field effect transistor, III-V

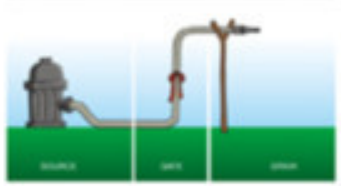
N5 / N3.5

Gate-all-around transistor



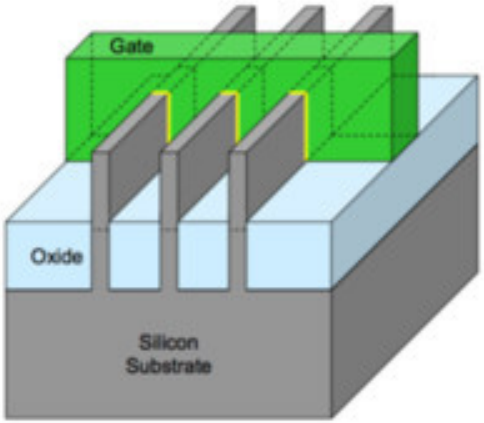




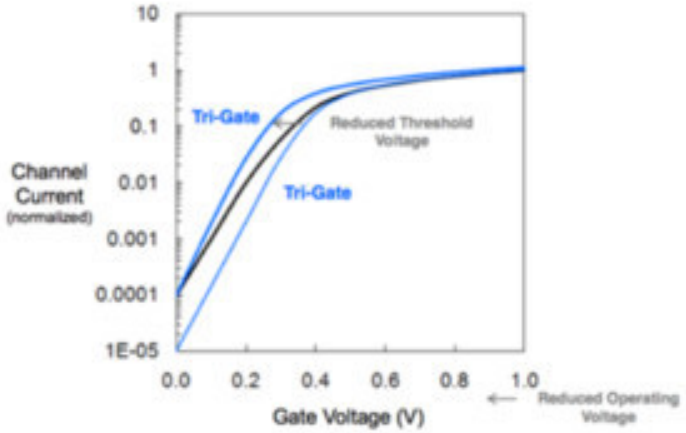


Source: ASML

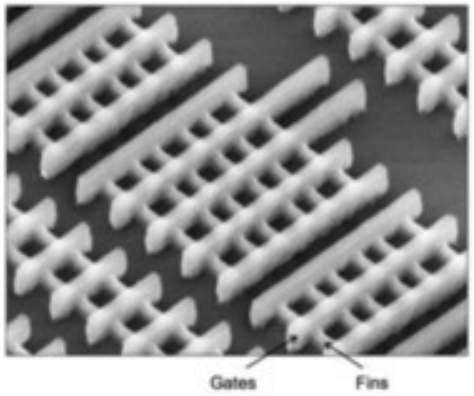
Transistor « Tri-Gate » (Intel)



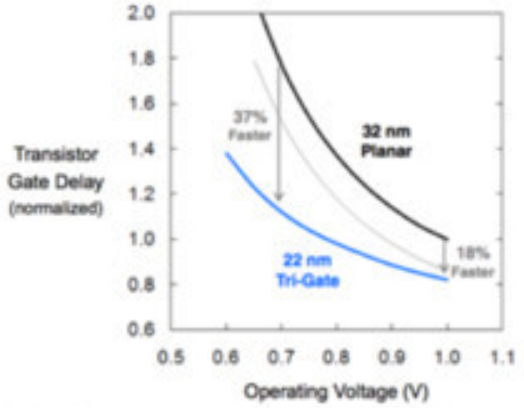
Transistor Operation



22 nm Tri-Gate Transistor



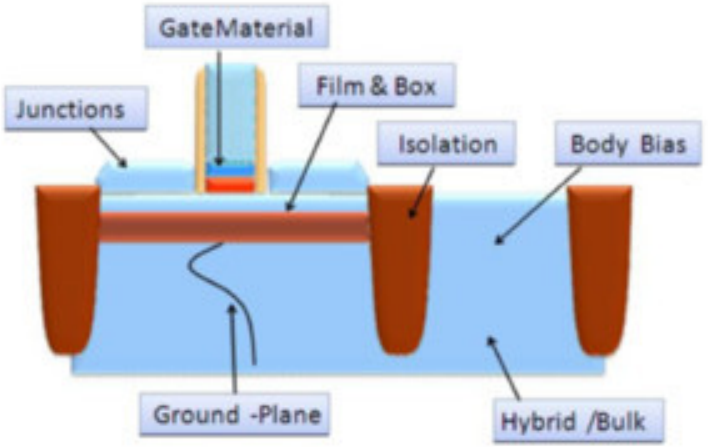
Transistor Gate Delay

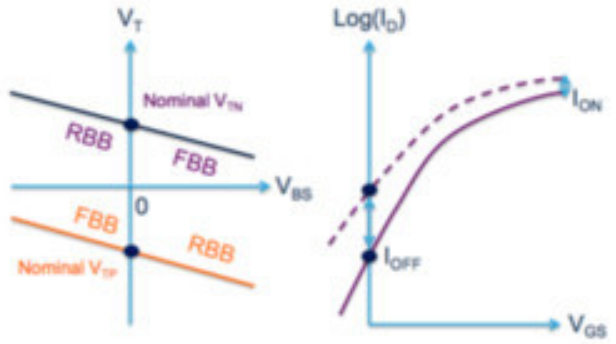


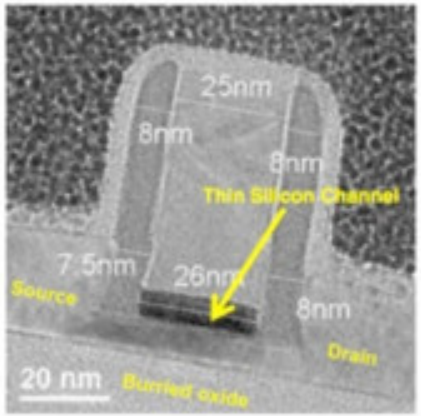
Source: Intel

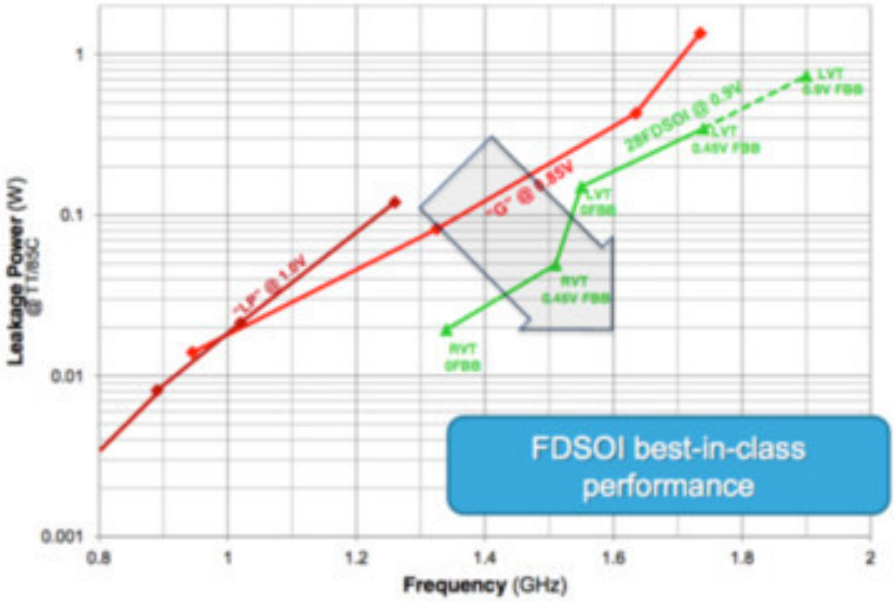
Transistor FD-SOI (STMicroelectronics)

UTBB-SOI : Ultra Thin Body (FD) and BOX SOI



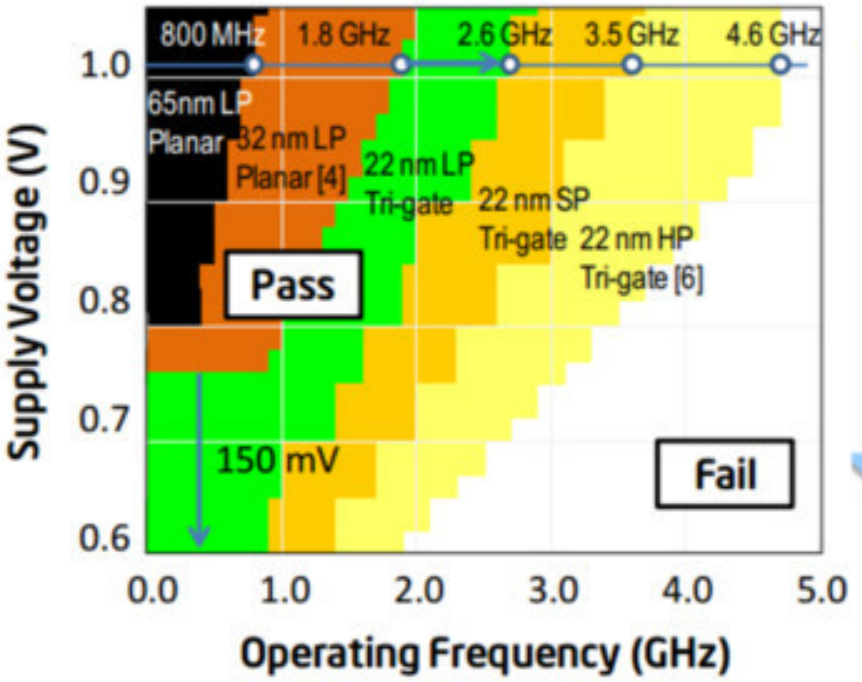


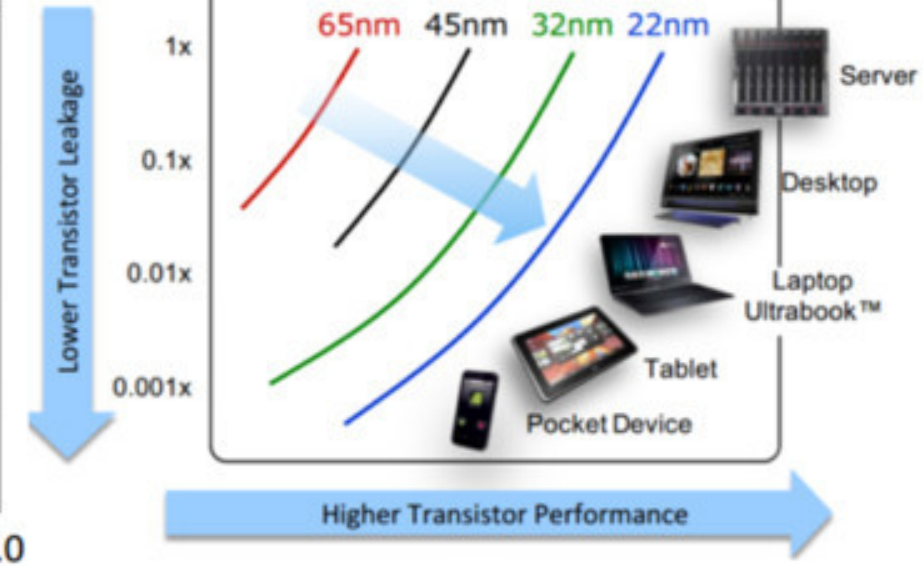




Source: STMicroelectronics

Architectures innovantes et nouveaux matériaux: « More Moore »



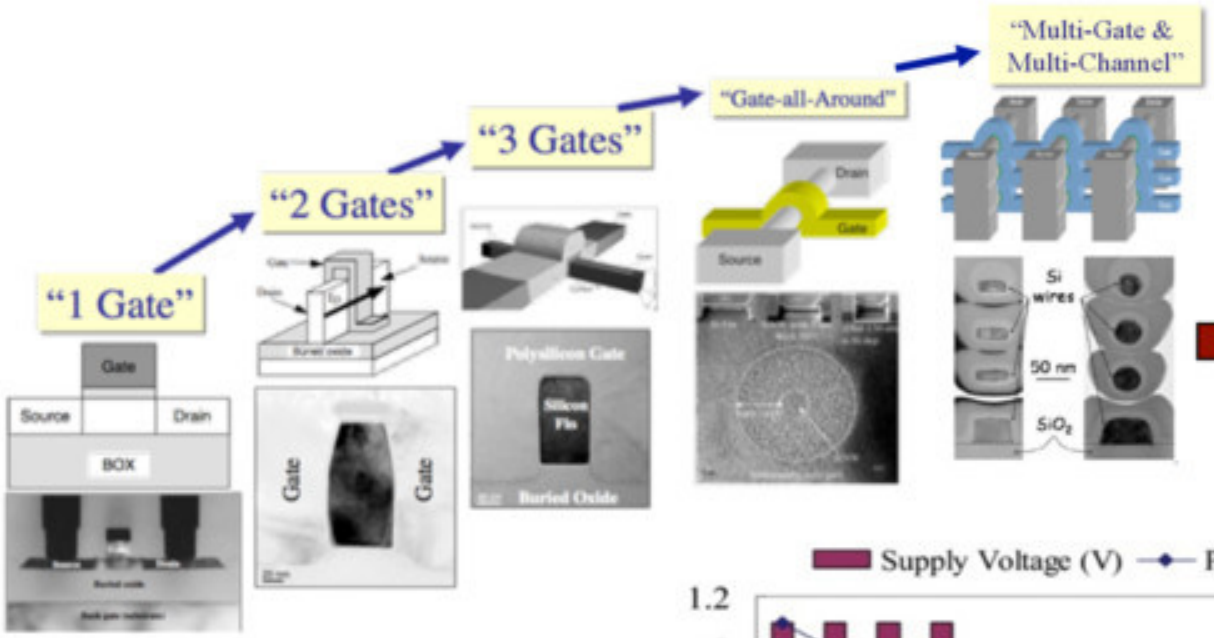


➔ Nano-architectures optimisées (électrostatique, transport)

➔ Gestion et optimisation de la consommation vs fréquence

➔ Augmentation de l'efficacité énergétique

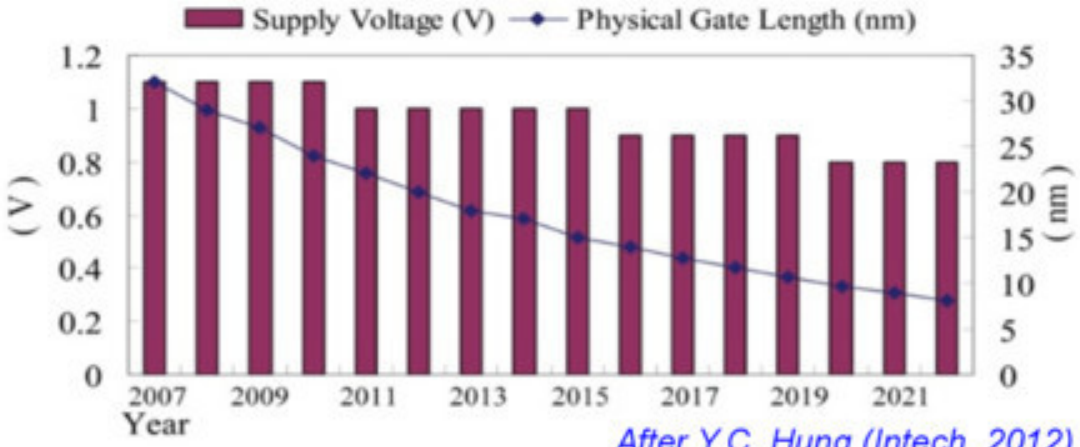
Architectures innovantes et nouveaux matériaux: « More Moore »



Combined with high mobility materials

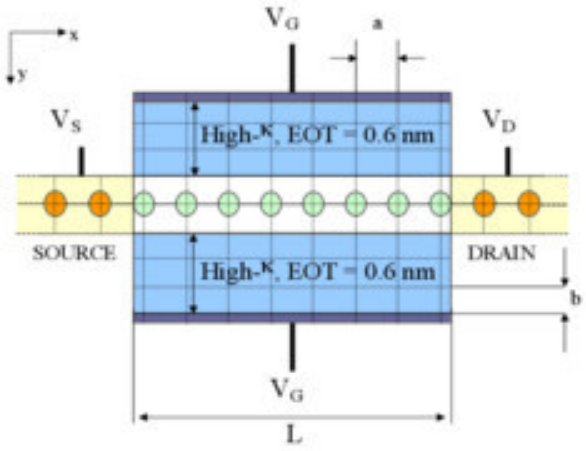
Ge
InP
GaAs
InAs
InGaAs

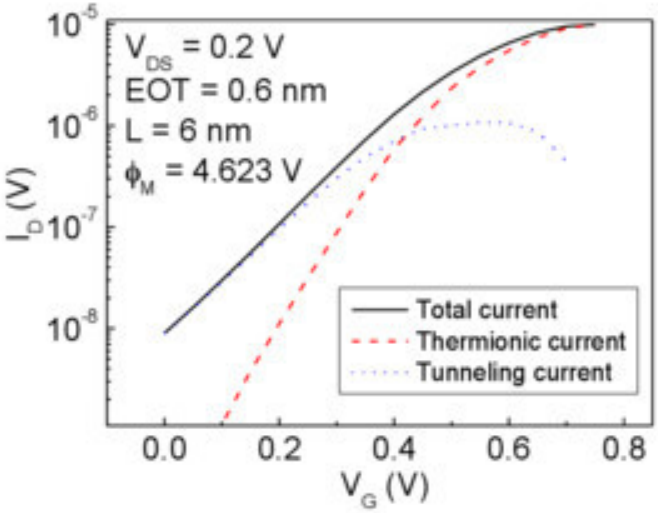
After Colinge (Tyndall)

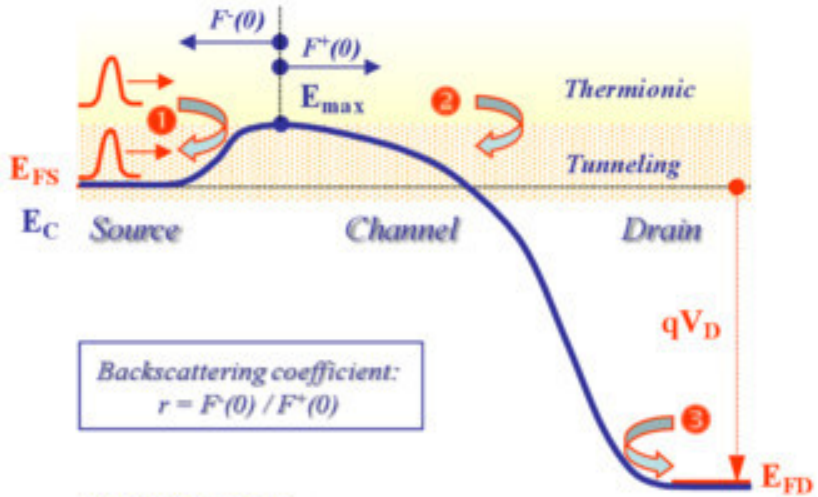


After Y.C. Hung (Intech, 2012)

Transistor MOS “ultime”: limites quantiques





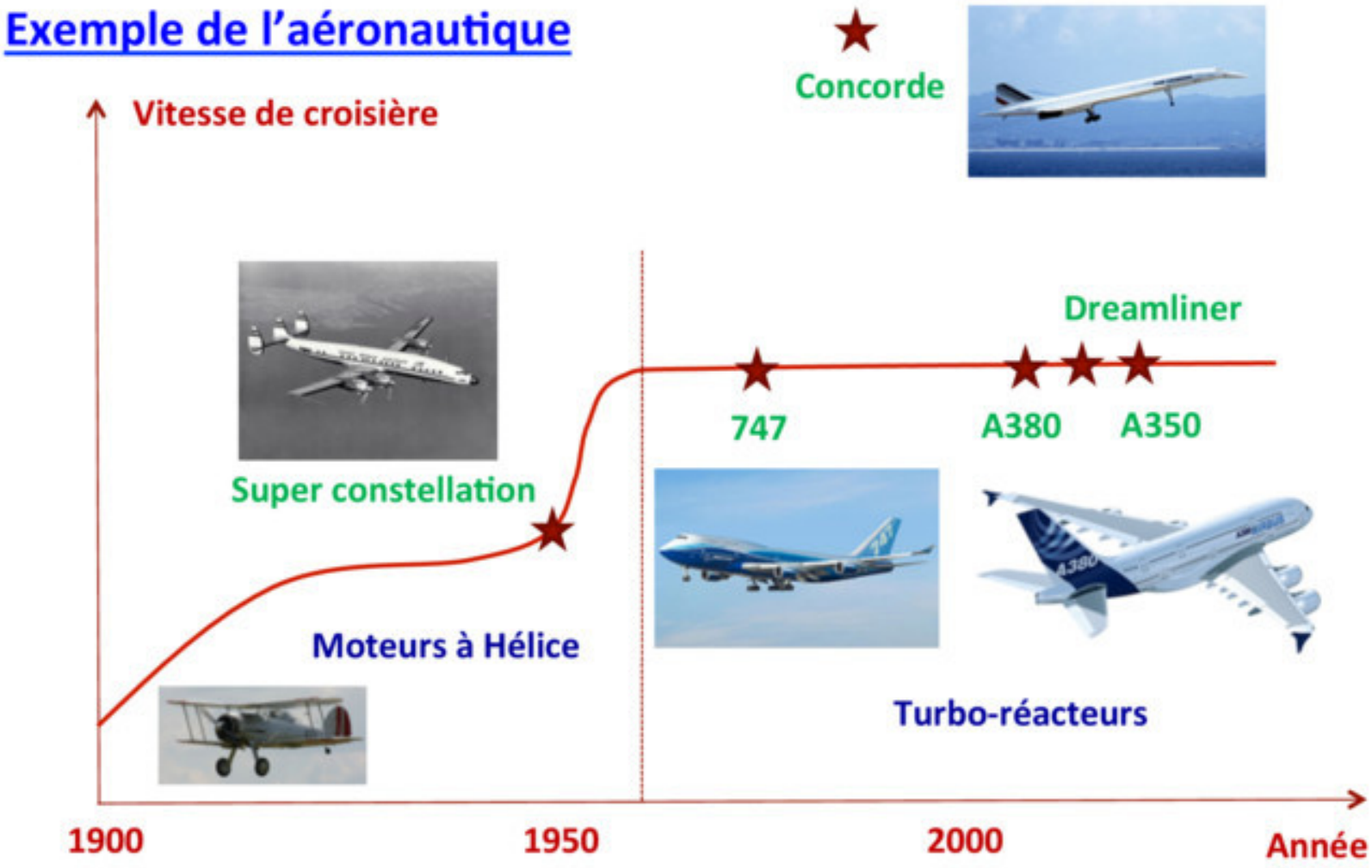


Year	2009	2011	2013	2015	2017	2019	2022
Physical gate length L (nm)	*20*	*16*	*13*	*10*	*8*	*6*	*4.5*
EOT (Å)	*10*	*8*	*6*	*6*	*5.5*	*5*	*5*
Si film thickness t_{Si} (nm)	*7*	*6*	*5*	*3*	*2*	*1.5*	*1*
Power supply voltage V_D (V)	*1.0*	*1.0*	*0.9*	*0.8*	*0.7*	*0.7*	*0.65*
R_{min} (%)	6.4	7.5	8.0	10	9.4	11.1	12.5
R_{max} (%)	54.0	54.0	52.3	50.5	47.1	47.1	47.1
R_{calc} (%)	***11.0***			***14.8***			***21.1***

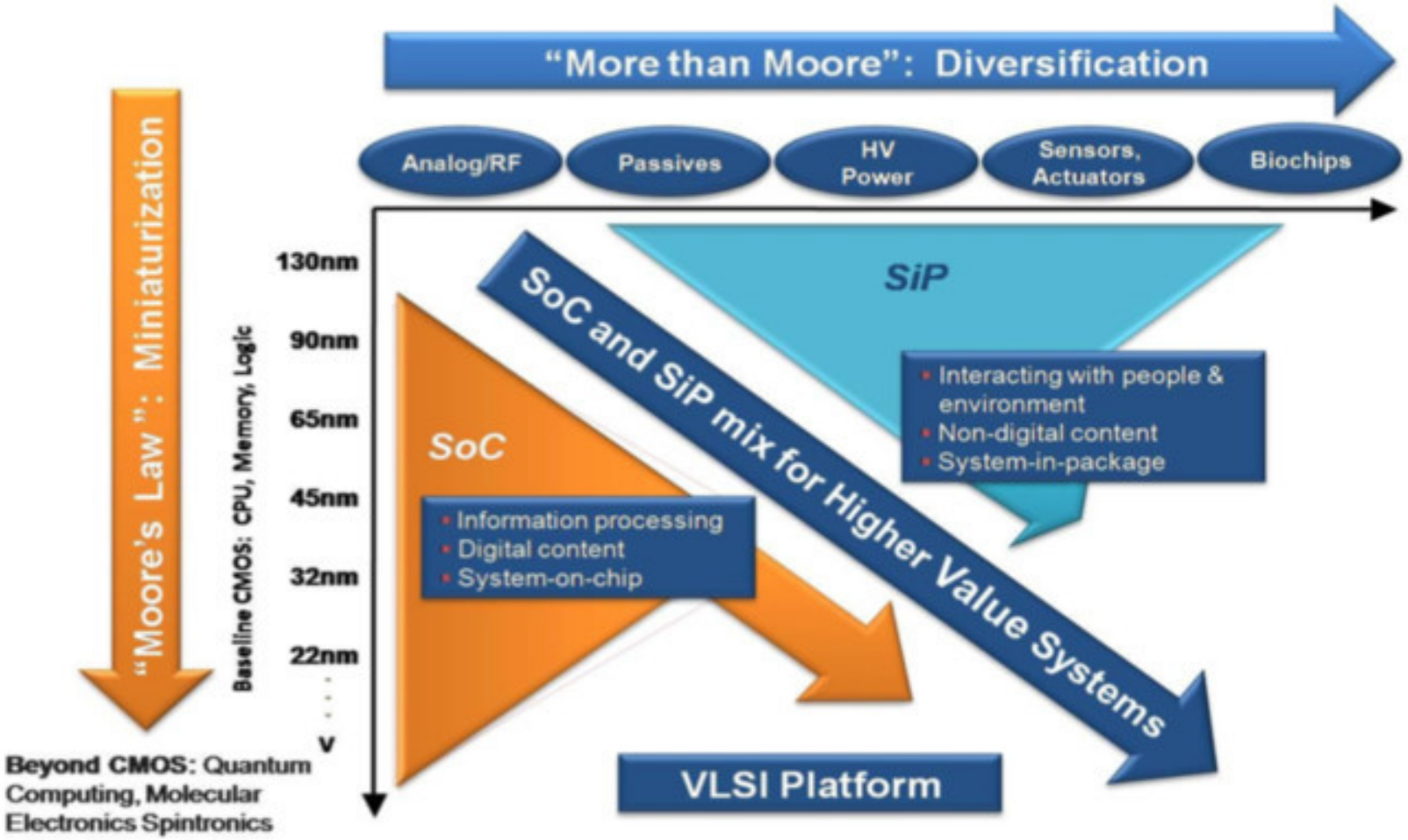
Source: IM2NP-CNRS

La fin de la microélectronique ?... Pas si sûr !!

Exemple de l'aéronautique

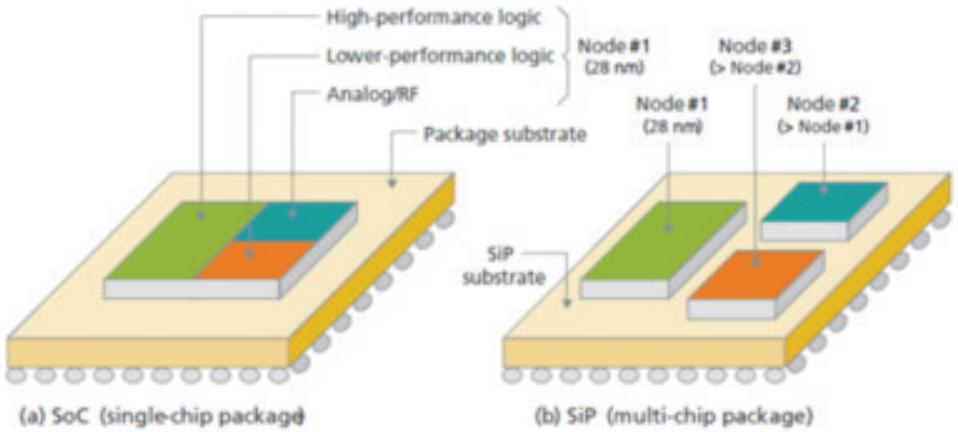


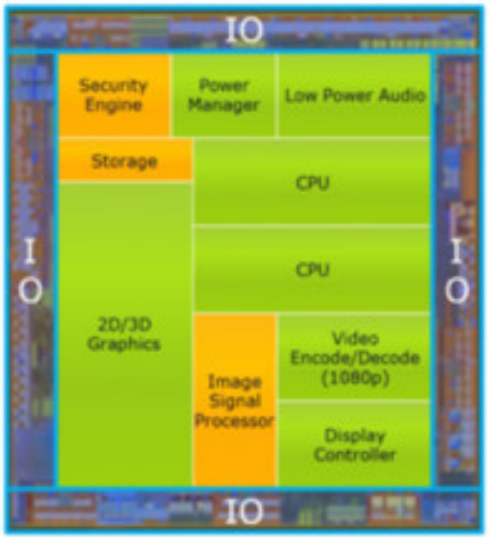
"More Moore" vs "More than Moore"

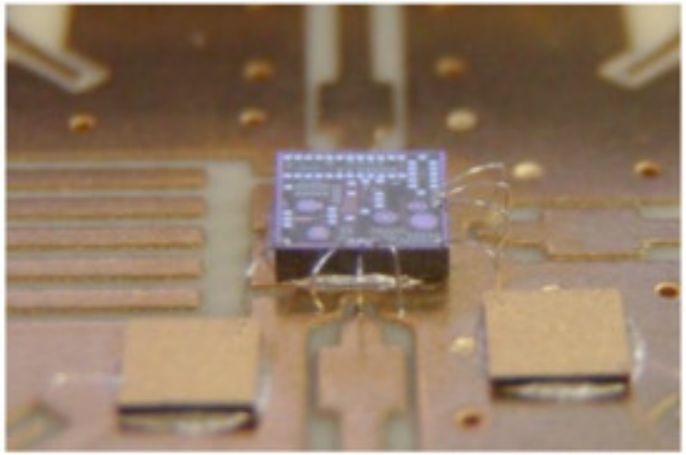


Source: STMicroelectronics

System-on-Chip (SoC) vs System-in-Package (SiP)





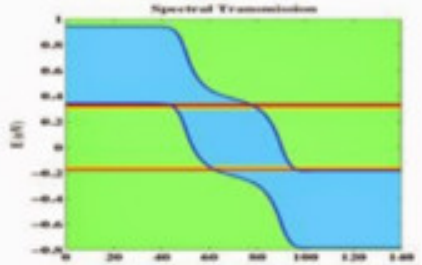


Source: IM2NP-CNRS

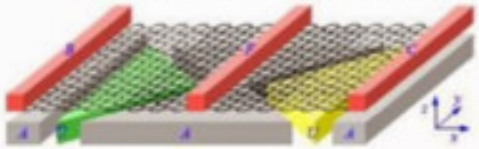
Beyond CMOS Devices

1. Electronic

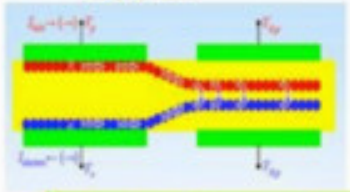
Tunneling FET



Graphene pn Junction

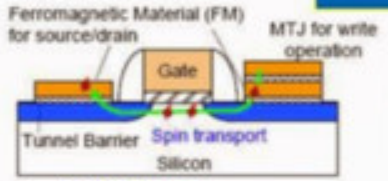


BisFET



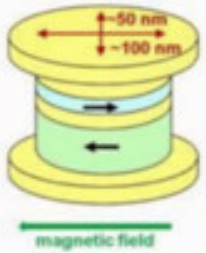
3. Orbitronic

2. Spintronic

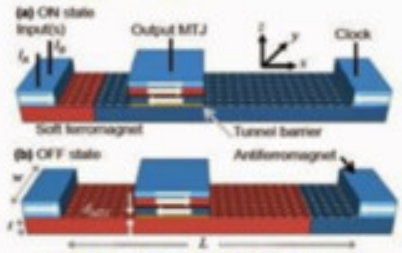


SpinFET

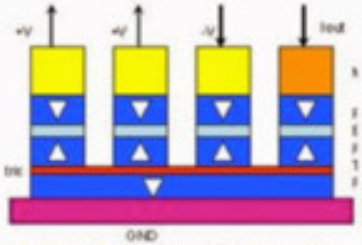
All Spin Logic



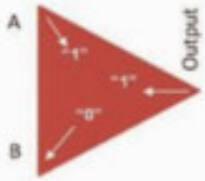
Spin Torque Oscillator



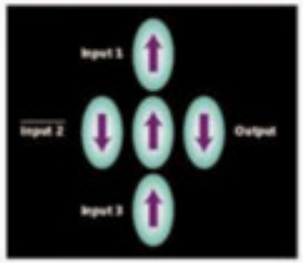
Domain Wall Logic



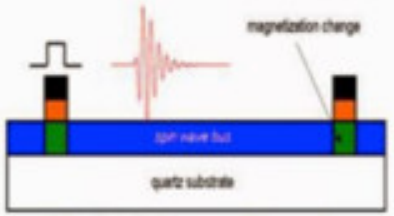
Spintronic Majority



Spin Torque Triad

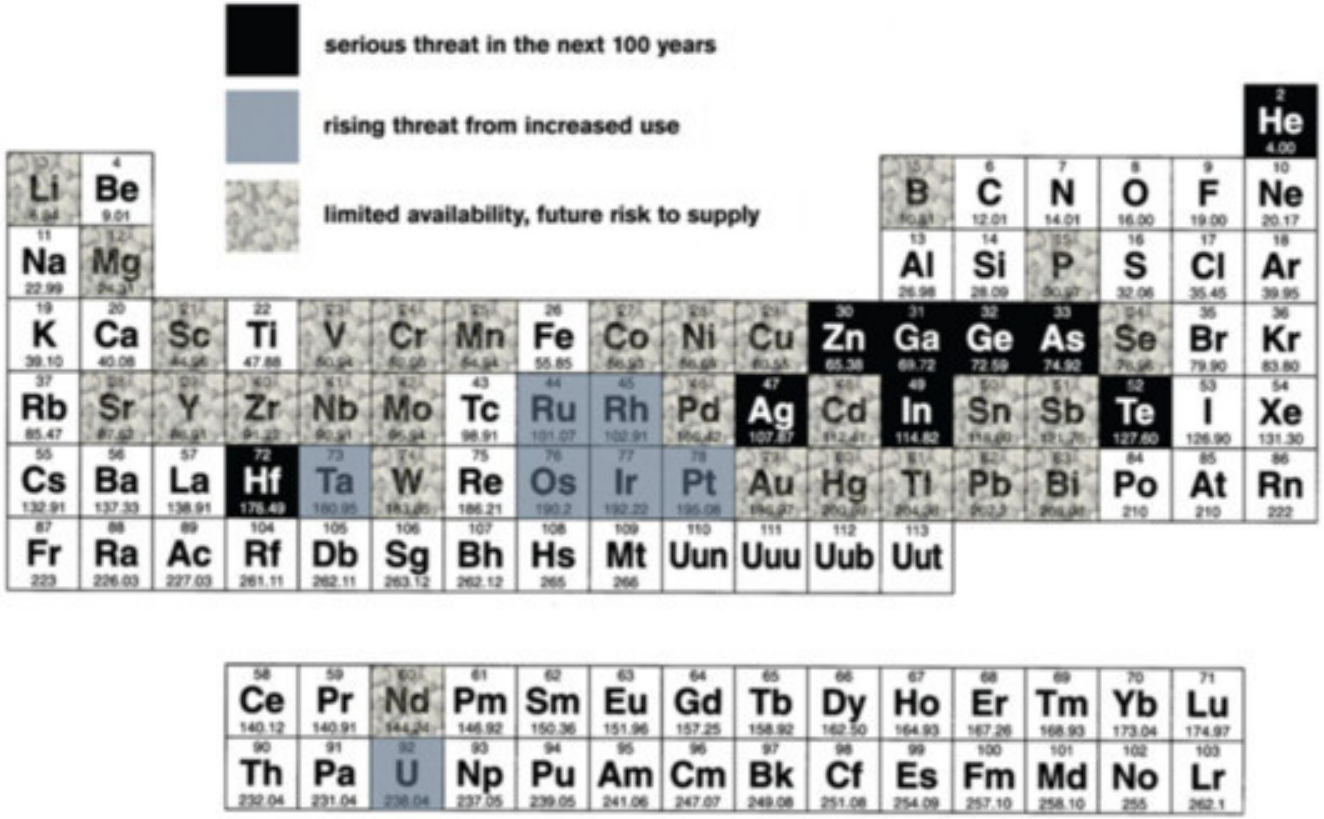


Nano Magnet Logic



Spin Wave Device

Criticité de certaines ressources naturelles ?



Source: Chemical Innovation

MERCI POUR VOTRE ATTENTION

Renseignements, contacts:

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jean-luc.autran@univ-amu.fr